Jonathan Fang

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Education

Georgia Institute of Technology — Atlanta, GA
M.S. Computer Science — *Aug. 2026 – May 2028*

University of Wisconsin-Madison — Madison, WI
B.S. Electrical and Computer Engineering — *May 2025*

- Relevant Classes: Microprocessor Systems, Digital System Design and Synthesis, Semiconductor Analysis, Artificial Intelligence, Computer Graphics, Compilers, Testable Design of Digital Systems

Technical Skills

Languages: C/C++, Python, SystemVerilog, Java, Bash, JavaScript
Tools: Linux (Ubuntu), Git, GDB, Jira, Quartus Prime, ModelSim, LTSpice, Altium, Oscilloscope, JTAG

Experience

Test Development Engineer — March 2026 – Present
Cisco · Product Operations — San Jose, CA

- Port and modernize manufacturing diagnostic tests for Catalyst 9400 switches across 3 board types into Cisco's current automated test framework, keeping factory test coverage consistent as boards move through production
- Validate and debug test sequences directly on hardware at production stations, partnering with the diagnostics team and CM engineers to resolve failures and keep manufacturing lines moving
- Connect product traceability data (serial numbers, assembly genealogy, cloud IDs) into the test flow to keep unit records aligned across the supply chain

Academic Tutor — Sept. 2025 – Jan. 2026
AJ Tutoring — Menlo Park, CA

- Managed caseload of 15 students across Algebra 2 Honors through Calculus, designing personalized curriculum and learning plans tailored to individual learning styles and academic goals

IT Technical Intern — Oct. 2023 – Dec. 2024
University of Wisconsin - Madison Department of Information Technology — Madison, WI

- Managed authentication infrastructure for 40,000+ users using Cisco ClearPass, maintaining 99.9% system uptime

Embedded Software Validation — June 2024 – Aug. 2024
Outlier — Remote

- Evaluated generated embedded C implementations for FPGA and microcontroller targets, assessing against real-time constraints, memory efficiency, and hardware limitations
- Validated embedded C implementations for STM32 microcontrollers, identifying memory leaks and timing violations

Embedded Research Lead — Sept. 2021 – May 2022
UW Transcend — Madison, WI

- Led 4-person team developing real-time FPGA-based image processing system, coordinating sprints and managing development pipeline using Jira and Agile methodology
- Optimized critical path timing to increase clock frequency from 125MHz to 150MHz (20% performance gain) while reducing FPGA resource utilization from 85% to 68%, validated through hardware testing protocols

Projects

PSoC6 Embedded Multiplayer Console | *C, FreeRTOS, SPI, I2C, UART*

- Designed modular game console platform with hot-swappable cartridges using FreeRTOS firmware architecture, enabling rapid game deployment across multiple titles
- Developed low-level device drivers for 16-bit LCD over SPI/I2C, integrating GPIO interrupts for precise system state management and real-time input handling

Partial Scan Test Design Optimization | *SystemVerilog, Synopsys, TetraMax, JTAG*

- Designed and optimized partial scan architecture for b14 benchmark circuit, achieving 46% improvement in test efficiency over full scan implementation while reducing chain length by 80%
- Reduced chip area by 7% through strategic circuit optimization while maintaining 41%+ fault detection coverage