Jonathan Fang

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Education

University of Wisconsin-Madison Madison, WI
B.S. Electrical and Computer Engineering *May. 2025*

- **Relevant Classes:** Microprocessor Systems, Digital System Design and Synthesis, Semiconductor Analysis, Artificial Intelligence, Computer Graphics, Compilers, Testable Design of Digital Systems

Technical Skills

Tools: Linux(Ubuntu), Git/Gitlab, GDB, Jira, Quartus Prime, ModelSim, LTSpice, Altium, Docker
Languages: C/C++, SystemVerilog, Java, Bash, Python, Javascript

Experience

UW Transcend Madison, WI
Embedded Research Lead *Sept 2021– May 2022*

- Co-led a team that was tasked with developing real-time image processing system on FPGA platform using SystemVerilog and Jira for Agile development
- Optimized critical path timing to increase clock frequency from 125MHz to 150MHz (20% performance gain) while reducing FPGA resource utilization from 85% to 68%, validated through hardware testing protocols

University of Wisconsin - Madison *Department of Information Technology* Madison, WI
IT Technical Intern *Oct 2023 - Dec 2024*

- Administered network authentication systems using Cisco ClearPass for 40k+ university users, gaining hands-on experience with large-scale user management systems and reliability
- Achieved 90% resolution rate managing 2000+ support tickets by implementing structured documentation protocols and establishing clear ownership workflows
- Provided technical consultation for hardware, diagnosing customer requirements and recommending appropriate hardware/software solutions to match use cases

Outlier Remote
Embedded Software Validation *June 2024– Aug 2024*

- Evaluated generated embedded C implementations for FPGA and microcontroller targets, assessing against real-time constraints, memory efficiency, and hardware limitations
- Documented system-level performance bottlenecks and edge cases in embedded deployments, analyzing resource constraints and real-time processing requirements

Projects

Infrared Sensor Fusion| SystemVerilog, FPGA, RTL Design

- Designed custom **SPI controller** for 6-axis IMU sensor interfacing with emphasis on signal integrity
- Implemented data-driven control systems using Python for algorithm testing and C for implementation, achieving <5% error through adaptive parameter tuning
- Developed **autonomous navigation system** for maze-solving robot integrating IMU sensor fusion with real-time path planning and boundary avoidance

PSoC6 Embedded Multiplayer Board| C, RTOS, I2C, UART

- Architected modular game console platform on PSoC6, enabling hot-swappable game modules through standardized firmware interface leveraging FreeRTOS task management and hardware abstraction layer
- Developed low-level device drivers for 16-bit LCD utilizing SPI protocol, integrating GPIO interrupts for precise **system state management**

Partial Scan Test Design Optimization| SystemVerilog, Synopsys, TetraMax, JTAG

- Designed and optimized partial scan architecture for b14 benchmark circuit, achieving 46% improvement in test efficiency metric over full scan implementation
- Performed ATPG and fault simulation using Synopsys TetraMAX, analyzing controllability and observability metrics to select scan flip-flops for optimal test coverage-to-area ratio **reducing chain length by 80%**